IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Y. Miyamoto et al.	: Art Unit:
Serial No.: To Be Assigned	: Examiner:
Filed: Herewith	:
FOR: ASYNCHRONOUS FIFO CIRCUIT AND METHOD OF READING AND WRITING DATA THROUGH ASYNCHRONOUS FIFO CIRCUIT	:

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

S I R :

Prior to examination, please amend the above-identified application as follows:

SPECIFICATION:

Specification at page 4, line 13:

One aspect of the present invention is an asynchronous FIFO circuit comprising:

Specification at page 5, line 10:

Another aspect of the present invention is an asynchronous FIFO circuit comprising:

Specification at page 7, line 3:

Still another aspect of the present invention is the asynchronous FIFO circuit, wherein said error write counter and said error read counter are formed of a gray code counter.